PROGRAMMING FLASH MEMORY VIA A BOUNDARY SCAN REGISTER

ABSTRACT

A method and parallel interface for on-board programming and/or In-System Configuration of a flash memory mounted on a printed circuit board by controlling its inputs with the aid of an ASIC mounted on the same circuit board via a Boundary Scan register of which the output signals are provided for activating or deactivating a write operation. The architecture description of the ASIC, flash memory, and the data format of the program and configuration data are stored in a Boundary-Scan Description Language file. The circuit board can be controlled via a JTAG interface suitable for performing function testing of the flash memory for input or output of standard bus signals and for input of the control signals of the ASIC. To reduce the programming effort, the data of the circuit diagram or of the network list derived from it is stored in the BSDL file.